IN THE CLAIMS

Claims 1-20 were pending. Claims 1, 4, 7, 10, 13, and 16 have been amended. Claims 3, 9, and 15 have been canceled without prejudice. Claims 1-2, 4-8, 10-14, and 16-20 remain pending. A complete list of claims is presented below with amendments marked up:

Current Listing of Claims

1. (Currently amended) A method comprising:

generating a first pixel stream on a first clock signal, the first clock signal being from a first source;

forwarding a second clock signal from a second source and the first pixel stream to a buffer to translate the first pixel stream into a second pixel stream on the second clock signal; and

providing a feedback to the second source to cause the second source to adjust the center frequency of the second clock signal to match the average frequency of the first clock signal with the average frequency of the second clock signal, wherein providing the feedback comprises

counting clock edges of the first clock signal,

counting clock edges of the second clock signal, and

sending a signal to the second source when clock edges of the first clock signal differ in number from clock edges of the second clock signal for a period of time.

2. (Original) The method of claim 1, wherein providing a feedback comprises sending a signal from the buffer to the second source when the content of the buffer reaches a predetermined threshold value.

3. (Canceled)

4. (Currently amended) The method of claim [[3]]1, wherein the second source includes a phase lock loop.

5. (Original) The method of claim 1, wherein the first clock signal is a non-spread spectrum modulation clock signal and the second clock signal is a spread spectrum modulation clock signal.

6. (Original) The method of claim 1, further comprising:

forwarding the first pixel stream to a cathode ray tube ("CRT") display; and

forwarding the second pixel stream to a liquid crystal display ("LCD") panel.

7. (Currently amended) An apparatus comprising:

a first circuitry to generate a first clock signal;

a display pipe being coupled to the first circuitry to receive the first clock signal and to generate a first pixel stream on the first clock signal;

a buffer being coupled to the display pipe to receive the first pixel stream and a second clock signal and to transform the first pixel stream into a second pixel stream on the second clock signal; ~~and~~

a second circuitry being coupled to the buffer to generate the second clock signal and to receive a feedback, wherein the second circuitry adjusts the center frequency of the second clock signal in response to the feedback; and

a counter being coupled to the first circuitry to count clock edges of the first clock signal and the second circuitry to count clock edges of the second clock signal, wherein the counter sends the feedback to the second circuitry when the clock edges of the first clock signal differ in number from the clock edges of the second clock signal for a period of time.

8. (Original) The apparatus of claim 7, wherein the buffer sends the feedback to the second circuitry when the buffer content reaches a predetermined threshold value.

9. (Canceled).

10. (Currently amended) The apparatus of claim [[9]]7, wherein the second circuitry comprises a phase lock loop.

11. (Original) The apparatus of claim 7, wherein the first clock signal is a non-spread spectrum modulation clock signal and the second clock signal is a spread spectrum modulation clock signal.

12. (Original) The apparatus of claim 7, wherein the first pixel stream is forwarded to a cathode ray tube ("CRT") display and the second pixel stream is forwarded to a liquid crystal display ("LCD") panel.

13. (Currently amended) A system comprising:

a dynamic random access memory ("DRAM");

a graphic memory controller hub being coupled to the DRAM, the graphic memory controller hub comprising

a first circuitry to generate a first clock signal;

a display pipe being coupled to the first circuitry to receive the first clock signal and to generate a first pixel stream on the first clock signal;

a buffer being coupled to the display pipe to receive the first pixel stream and a second clock signal and to transform the first pixel stream into a second pixel stream on the second clock signal; ~~and~~

a second circuitry being coupled to the buffer to generate the second clock signal and to receive a feedback, wherein the second circuitry adjusts the center frequency of the second clock signal in response to the feedback; and

a counter being coupled to the first circuitry to count clock edges of the first clock signal and the second circuitry to count clock edges of the second clock signal, wherein the counter sends the feedback to the second circuitry when the clock edges of the first clock signal differ in number from the clock edges of the second clock signal for a period of time.

14. (Original) The system of claim 13, wherein the buffer sends the feedback to the second circuitry when the buffer content reaches a predetermined threshold value.

15. (Canceled).

16. (Currently amended) The system of claim ~~15~~ 13, wherein the second circuitry comprises a phase lock loop.

17. (Original) The system of claim 13, wherein the first clock signal is a non-spread spectrum modulation clock signal and the second clock signal is a spread spectrum modulation clock signal.

18. (Original) The system of claim 13 further comprising a liquid crystal display ("LCD") panel being coupled to the graphic memory controller hub to receive the second pixel stream.

19. (Original) The system of claim 18, wherein the first pixel stream is forwarded to a cathode ray tube ("CRT") display.

20. (Original) The system of claim 13 further comprising a processor being coupled to the graphic memory controller hub.